384kHz Stereo Audiophile Performance D/A Converter

Features

- Discrete implementation of DAC
- Proprietary digital upsampling algorithms with transient conserving response
- PCM inputs up to 384kHz / 24 bits
- DSD input up to 11.2MHz
- All inputs are up-converted to 128FS sample rate before being converted to analog (except DSD 4X)
- Integrated AES/EBU decoder also supports DoP for DSD 1X
- Integrated I2S receiver supports all PCM and DSD format (DoP and direct DSD on I2S)
- Integrated re-clocking algorithm designed to reject jitter on incoming digital audio signals
- Master or slave clock operation (8FS PCM and DSD 4X only supported in master mode).
- Dual differential analog output filters designed with the same goals in transient behavior as the digital upsampling filters
- Integrated analog line stage, dual differential
- 2 separate analog outputs after each analog filter for external line stage
- +/- 12VA and 8VD operation
- A unique feature allows the host to update the firmware of the ADM module by playing a specially formatted audio file into the module.

General Description

The ADM module is an audiophile grade D/A converter for the most demanding applications, where standard off-the-shelf chip solutions are not good enough. All components and algorithms have been designed discretely with internal precision of 72 bits and the goal to treat transient characteristics in the music signal like only analog audio equipment does. The result of this novel design concept is the most “analog like” system in digital audio.

The module can receive digital audio directly in AES/EBU, I2S or DSD format, which then are all upsampled to 128FS 1-bit delta-sigma through a proprietary algorithm that, unlike standard digital filters, varies its characteristics in time to safeguard the transient nature of music signals. A final digital processing step further increases the data rate by a factor of 4 and readies the signal for the discrete analog low-pass filter and low impedance output line stage.

The ADM also contains a clock generator that is only very loosely connected to the incoming digital audio stream to reject any clock jitter from those signals. No PLL is used. Part of this clock generator is a small buffer for the audio data.

DSD 2X is only supported on the I2S input.

8FS PCM and DSD 4X data formats are only supported on the I2S input and also only in clock master mode.

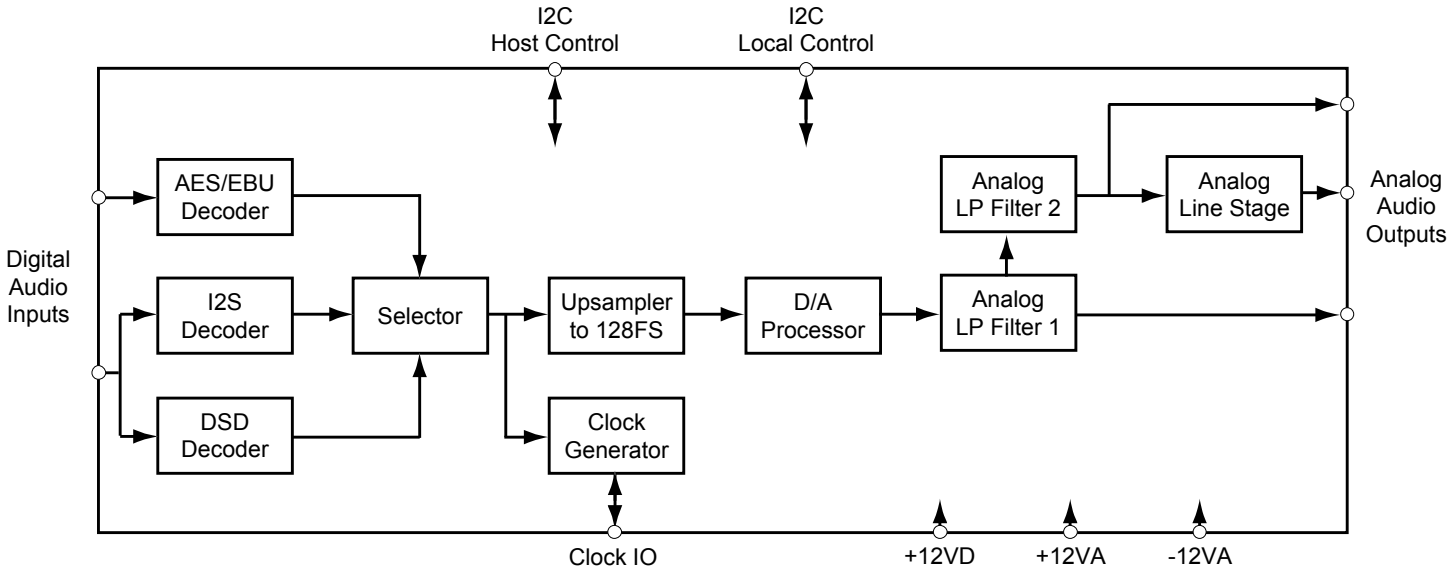


Figure 1

Pinouts

At the bottom of the module there are 4 connectors for all digital and analog signals and power supplies:

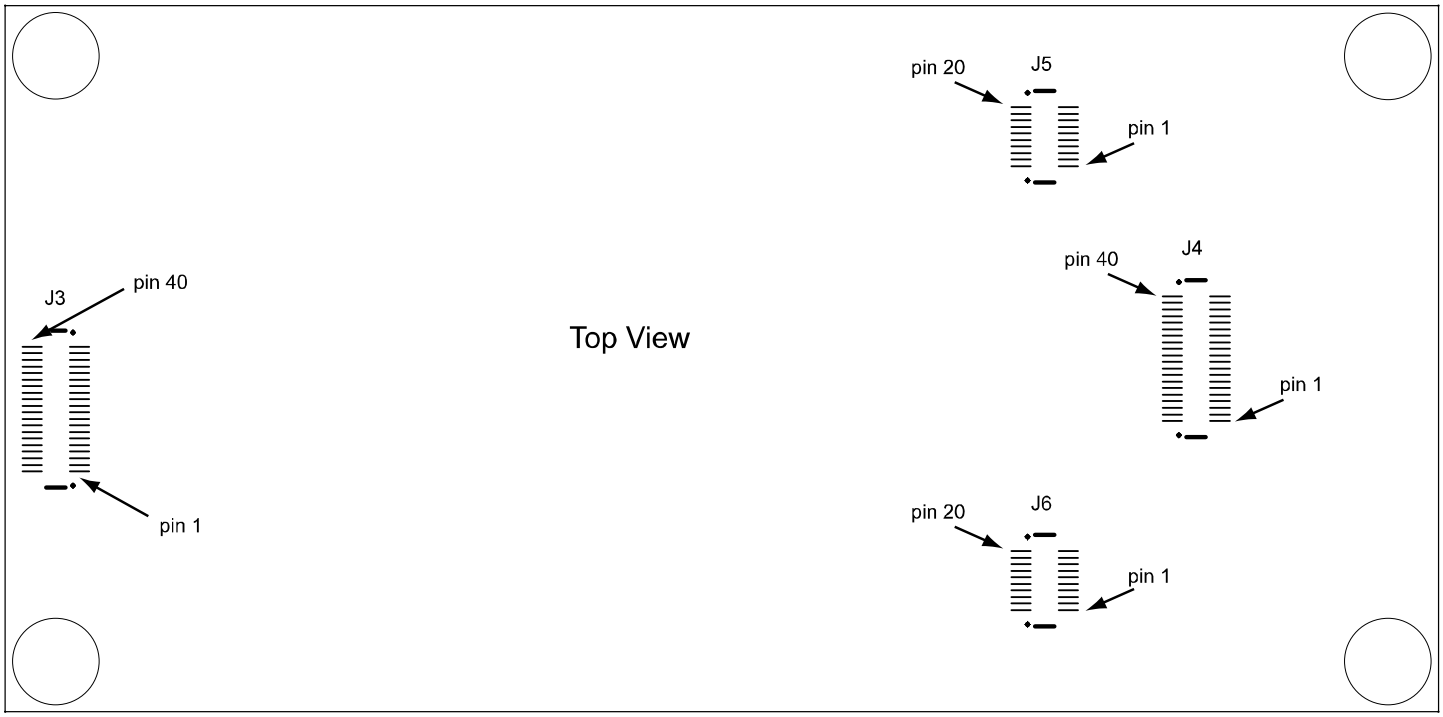


Figure 2

J3 Digital Signals

Connector type: Samtec LSS-120-03-F-DV-A-K
Mating connector type: Samtec LSS-120-03-F-DV-A-K
All signal levels are TTL compatible, referenced to 3.3V and **no signal input is 5V tolerant.**

Pin	Signal	Direction	Description
1	NC		Used for test, do not connect
2	NC		Used for test, do not connect
3	DGND		Digital Ground
4	DGND		Digital Ground
5	NC		Used for test, do not connect
6	NC		Used for test, do not connect
7	I2C_A1	in	Address bit 1 for I2C host bus
8	I2C_A0	in	Address bit 0 for I2C host bus
9	SDA_HOST	in/out	SDA of host I2C bus, needs external 3V3 pull-up resistors, not 5V tolerant
10	SDA_LOC	in/out	SDA of local I2C bus, 3V3 pull-up resistors on module, not 5V tolerant
11	SCL_HOST	in	SCL of host I2C bus, needs external 3V3 pull-up resistors, not 5V tolerant
12	SCL_LOC	out	SCL of local I2C bus, 3V3 pull-up resistors on module, not 5V tolerant
13	DGND		Digital Ground
14	DGND		Digital Ground
15	SEL_INT	in	set 1 to select master clock operation

			set 0 to select slave clock operation
16	xMUTE	in	Mute signal, active low, internal pull-up resistor
17	NC		Used for test, do not connect
18	xINIT	in	Reset signal, active low, internal pull-up resistor, hold low for >1s during power up
19	DGND		Digital Ground
20	DGND		Digital Ground
21	I2S_DAT	in	I2S data input. When SEL_DSD=0 then L/R PCM data, else DSD left channel data, maximum of 384kHz sample rate for PCM is supported
22	AES_IN	in	AES/EBU input, maximum of 192kHz sample rate is supported
23	I2S_LRCK	in	When SEL_DSD=0 then L/R clock, else DSD right channel data
24	I2S_BCK	in	I2S bit clock input, 2x24 or 2x32 cycles per L/R sample for PCM, 2.8224MHz for DSD, 5.6448MHz for DSD 2X, 11.2896MHz for DSD 4X
25	NC		Used for test, do not connect
26	NC		Used for test, do not connect
27	SEL_DSD	in	0 when I2S input is used for PCM data 1 when I2S input is used for DSD data
28	SEL_I2S	in	0 to select AES_IN as digital audio input 1 to select I2S input
29	SEL_44	in	set 1 to select multiples of 44.1kHz sample rate in master clock operation, set 0 to select multiples of 48kHz sample rate in master clock operation, ignored during slave clock operation.
30	xMUTE_RLY	out	Active low signal to control analog output relays, 0 when output needs to be muted
31	MCK	out	512FS master clock
32	NC		Used for test, do not connect
33	DGND		Digital Ground
34	DGND		Digital Ground
35	+3V3	out	+3.3V output, 100mA max.
36	VD	in	Digital supply voltage
37	VD	in	Digital supply voltage
38	VD	in	Digital supply voltage
39	DGND		Digital Ground
40	DGND		Digital Ground

J4 Analog Line Stage Signals

Connector type: Hirose Samtec LSS-120-03-F-DV-A-K
Mating connector type: Samtec LSS-120-03-F-DV-A-K

Pin	Signal	Direction	Description
1	AGND		Analog Ground
2	AGND		Analog Ground
3	LS_AUDIO_L-	out	Analog line stage audio output, left channel -
4	LS_AUDIO_L+	out	Analog line stage audio output, left channel +
5	LS_AUDIO_L-	out	Analog line stage audio output, left channel -
6	LS_AUDIO_L+	out	Analog line stage audio output, left channel +
7	LS_AUDIO_L-	out	Analog line stage audio output, left channel -
8	LS_AUDIO_L+	out	Analog line stage audio output, left channel +
9	AGND		Analog Ground
10	AGND		Analog Ground
11	AGND		Analog Ground
12	AGND		Analog Ground

13	AGND		Analog Ground
14	AGND		Analog Ground
15	AGND		Analog Ground
16	AGND		Analog Ground
17	VA_N		Negative analog supply voltage
18	VA_P		Positive analog supply voltage
19	VA_N		Negative analog supply voltage
20	VA_P		Positive analog supply voltage
21	VA_N		Negative analog supply voltage
22	VA_P		Positive analog supply voltage
23	VA_N		Negative analog supply voltage
24	VA_P		Positive analog supply voltage
25	AGND		Analog Ground
26	AGND		Analog Ground
27	AGND		Analog Ground
28	AGND		Analog Ground
29	AGND		Analog Ground
30	AGND		Analog Ground
31	AGND		Analog Ground
32	AGND		Analog Ground
33	LS_AUDIO_R-	out	Analog line stage audio output, right channel -
34	LS_AUDIO_R+	out	Analog line stage audio output, right channel +
35	LS_AUDIO_R-	out	Analog line stage audio output, right channel -
36	LS_AUDIO_R+	out	Analog line stage audio output, right channel +
37	LS_AUDIO_R-	out	Analog line stage audio output, right channel -
38	LS_AUDIO_R+	out	Analog line stage audio output, right channel +
39	AGND		Analog Ground
40	AGND		Analog Ground

J5 Analog Pre-Line Stage Signals for Left Channel

Connector type: Samtec LSS-110-03-F-DV-A-K
Mating connector type: Samtec LSS-110-03-F-DV-A-K

Pin	Signal	Direction	Description
1	AGND		Analog Ground
2	AGND		Analog Ground
3	PL1_AUDIO_L-	out	Analog audio output after 1st filter before line stage, left channel -, (voltage source)
4	PL1_AUDIO_L+	out	Analog audio output after 1st filter before line stage, left channel +, (voltage source)
5	PL1_AUDIO_L-	out	Analog audio output after 1st filter before line stage, left channel -, (voltage source)
6	PL1_AUDIO_L+	out	Analog audio output after 1st filter before line stage, left channel +, (voltage source)
7	PL1_AUDIO_L-	out	Analog audio output after 1st filter before line stage, left channel -, (voltage source)
8	PL1_AUDIO_L+	out	Analog audio output after 1st filter before line stage, left channel +, (voltage source)
9	AGND		Analog Ground
10	AGND		Analog Ground
11	AGND		Analog Ground
12	AGND		Analog Ground
13	PL2_AUDIO_L-	out	Analog audio output after 2nd filter before line stage, left channel -, (voltage source)
14	PL2_AUDIO_L+	out	Analog audio output after 2nd filter before line stage, left channel +, (voltage source)
15	PL2_AUDIO_L-	out	Analog audio output after 2nd filter before line stage, left channel -, (voltage source)
16	PL2_AUDIO_L+	out	Analog audio output after 2nd filter before line stage, left channel +, (voltage source)

17	PL2_AUDIO_L-	out	Analog audio output after 2nd filter before line stage, left channel -, (voltage source)
18	PL2_AUDIO_L+	out	Analog audio output after 2nd filter before line stage, left channel +, (voltage source)
19	AGND		Analog Ground
20	AGND		Analog Ground

J6 Analog Pre-Line Stage Signals for Right Channel

Connector type: Samtec LSS-110-03-F-DV-A-K
Mating connector type: Samtec LSS-110-03-F-DV-A-K

Pin	Signal	Direction	Description
1	AGND		Analog Ground
2	AGND		Analog Ground
3	PL1_AUDIO_R-	out	Analog audio output after 1st filter before line stage, right channel -, (voltage source)
4	PL1_AUDIO_R+	out	Analog audio output after 1st filter before line stage, right channel +, (voltage source)
5	PL1_AUDIO_R-	out	Analog audio output after 1st filter before line stage, right channel -, (voltage source)
6	PL1_AUDIO_R+	out	Analog audio output after 1st filter before line stage, right channel +, (voltage source)
7	PL1_AUDIO_R-	out	Analog audio output after 1st filter before line stage, right channel -, (voltage source)
8	PL1_AUDIO_R+	out	Analog audio output after 1st filter before line stage, right channel +, (voltage source)
9	AGND		Analog Ground
10	AGND		Analog Ground
11	AGND		Analog Ground
12	AGND		Analog Ground
13	PL2_AUDIO_R-	out	Analog audio output after 2nd filter before line stage, right channel -, (voltage source)
14	PL2_AUDIO_R+	out	Analog audio output after 2nd filter before line stage, right channel +, (voltage source)
15	PL2_AUDIO_R-	out	Analog audio output after 2nd filter before line stage, right channel -, (voltage source)
16	PL2_AUDIO_R+	out	Analog audio output after 2nd filter before line stage, right channel +, (voltage source)
17	PL2_AUDIO_R-	out	Analog audio output after 2nd filter before line stage, right channel -, (voltage source)
18	PL2_AUDIO_R+	out	Analog audio output after 2nd filter before line stage, right channel +, (voltage source)
19	AGND		Analog Ground
20	AGND		Analog Ground

RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Min.	Typ.	Max.	Units
Digital power supply	VD	+7	+8	+9	V
Ramp up time from GND to VD	VD			100	ms
Positive analog power supply	VA_P	+10.5	+12	13	V
Negative analog power supply	VA_N	-10.5	-12	-13	V
All digital signal input levels (TTL compatible)			3.3	3.75	V
Digital supply current	I_{VD}		500	700	mA
Analog supply current VA_P	I_{VA_P}		100	150	mA
Analog supply current VA_N	I_{VA_N}		100	150	mA
Ambient temperature	T_A	-10		+45	°C

ANALOG CHARACTERISTICS (MAIN LINE STAGE OUTPUT)

(T_A = 25°C; VD=+12V, VA_P=+12V, VA_N=-12V; full-scale input sinewave, 997Hz)

Description	Min.	Typ.	Max.	Units
Total Harmonic Distortion + Noise (<10Hz to 30kHz)		0.005	0.01	%
DC offset	0	<4	10	mV
Output signal voltage, differential, peak-to-peak		9		V
Output impedance		22		Ω

ANALOG CHARACTERISTICS (PRE-OUT AFTER 1st ANALOG FILTER)

(T_A = 25°C; VD=+12V, VA_P=+12V, VA_N=-12V; full-scale input sinewave; Measurement bandwidth is 0Hz to 30kHz)

Parameter	Condition	Value	Units
Differential output level (peak-to-peak)	0dBFS	2.3	V
Output impedance	DC to 10kHz	<10	Ω
THD+N	0dBFS, 1kHz	<0.012	%
Load impedance		>=600	Ω

ANALOG CHARACTERISTICS (PRE-OUT AFTER 2nd ANALOG FILTER)

(T_A = 25°C; VD=+12V, VA_P=+12V, VA_N=-12V; full-scale input sinewave; Measurement bandwidth is 0Hz to 30kHz)

Parameter	Condition	Value	Units
Differential output level (peak-to-peak)	0dBFS	4.6	V
Output impedance	DC to 10kHz	<10	Ω
THD+N	0dBFS, 1kHz	<0.005	%
Load impedance		>=600	Ω

SWITCHING CHARACTERISTICS

Description	Min.	Typ.	Max.	Units
MCK Frequency		512		FS[1)]
Duty cycle of AES/EBU input signal		50/50		%
Host I2C Bus				
SCL Clock Frequency			100	kHz
SDA setup time before postive edge of SCL	100			ns
SDA hold time after negative edge of SCL		0		ns
Local I2C Bus				
SCL Clock Frequency		0.5		FS

1) FS=44.1kHz or 48kHz.

GENERAL DESCRIPTION

Power-up and Reset
At power-up the ADM automatically loads the software from an internal flash memory. As this process takes about 700ms from the time the digital power supply reached its nominal value, the active low xINIT pulse needs to be held low for at least 1s to make sure all registers are initialized correctly. Incorrect initialization will result in sonic degradation.

AES/EBU receiver
The ADM has an integrated AES/EBU receiver from which it extracts the sample rate information. All sample rate switching is automatic and for that reason it is important that the AES/EBU signal has exactly a 50/50% duty cycle as it reaches the input of the module, or else the sample rates mostly around 4FS cannot be detected reliably.
Sample rates of all multiples of 44.1kHz and 48kHz up to 192kHz are supported. The AES/EBU receiver is selected when the signal SEL_I2S is low.
DSD via DoP is supported for DSD 1X only.

I2S receiver
The I2S receiver works very similarly to the AES/EBU receiver. The ADM directly extracts all sample rate information from the input signals and adjusts the algorithms accordingly.
The 3 signal lines (I2S_DAT, I2S_BCK, I2S_LRCK) also double as DSD inputs, where I2S_DAT becomes the data input for the left channel, the I2S_LRCK becomes the data input for the right channel and I2S_BCK is the 64FS, 128FS or 256FS bit clock.
The I2S receiver is selected when the signal SEL_I2S is high. In addition the signal SEL_DSD selects DSD input when high or PCM input when low.
For PCM inputs the I2S_BCK can have either 2 times 24 cycles per Left/Right sample or 2 times 32 cycles. The I2S receiver will automatically detect the number of clock cycles and receive the data correctly either way.
DoP is supported for DSD up to 4X.
NOTE: 8FS PCM and DSD 4X formats are only supported in clock master mode.

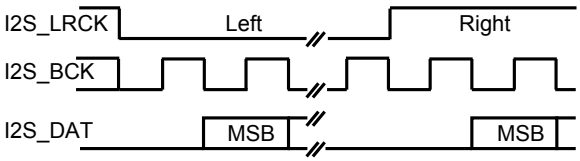


Figure 3
Timing for I2S receiver in PCM mode

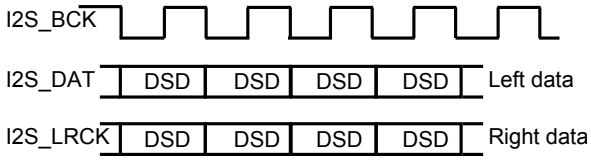


Figure 4
Timing for I2S receiver in DSD mode

DSD-over-PCM (DoP)
DoP is an open industry standard that was created to allow the transmission of DSD data over standard PCM interfaces such as AES/EBU, I2S or USB etc. For this 16 DSD bits are packed into a 24-bit PCM frames. The remaining 8 bits in the frame are used as a marker to signal the compliant receiver that the contained data is DSD. Details of the standard can be found in the standard which can be downloaded from our website: www.akdesigninc.com.
The standard is supported in both digital input receivers, AES/EBU and I2S.

Clock Generator
The clock generator can operate in either master (internal) or in slave (external) mode. In master mode the master clock output (MCK) can be used to send a word clock back to the digital source. In this mode the fundamental FS frequency needs to be selected via the signal SEL_44. In slave mode the clock generator extracts the sample rate information from the selected audio input through a proprietary algorithm that locks the internal master clock only very loosely to the sample rate in order to minimize any clock jitter on the digital audio input signal. No PLL (phase-locked –loop) is used as they generally are not adequate to filter jitter enough for high quality sonic performance. Even though the audio data is buffered the delay is very short and lock condition is achieved nearly instantly (faster than with a PLL).
NOTE: when switching the fundamental FS frequency (via SEL_44) in master mode the ADM generates an internal reset and the xMUTE_RLY output signal that can be used to close output relays during the change of frequency.

Upsampling algorithm
All decoded PCM and DSD inputs are upsampled to 128FS 1-bit delta-sigma before being processed for analog conversion, except for DSD 4X inputs which are converted to analog directly. 1FS PCM inputs are first upsampled to 2FS through an unique algorithm that is constantly adjusted depending on the transient behavior of the underlying music signal. Similarly, 2FS and 4FS

PCM signals are upsampled to 16FS before being converted to 128FS 1-bit delta-sigma. This conversion process allows short transients to be converted correctly, unlike in most other converters that generate pre-ringing effects that are generally described by audiophiles as “digital harshness”. This proprietary algorithm results in an “analog like” sonic performance.
The following graphs illustrate this characteristic, where the pre- and post-ringing effects of common algorithms are completely eliminated in the ADM module.
DSD input signals at 64FS are first lowpass filtered to limit their inherent high frequency noise, and then converted to 128FS 1-bit delta-sigma. This operation is performed in the DSD domain without any conversion to PCM.

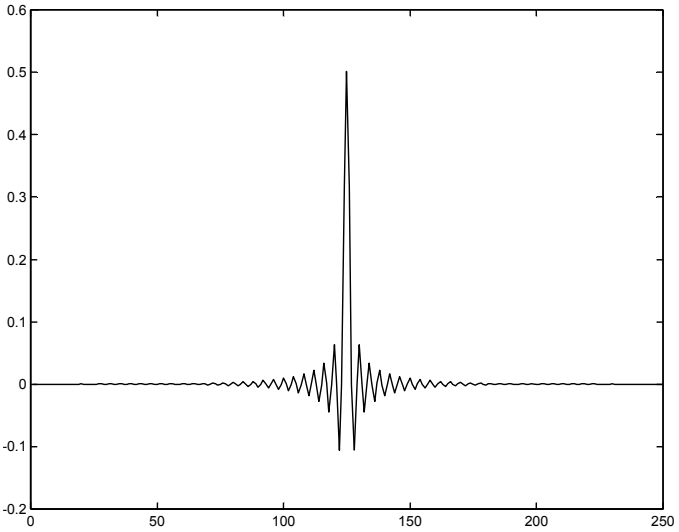


Figure 5
Typical impulse response of a standard upsampling filter

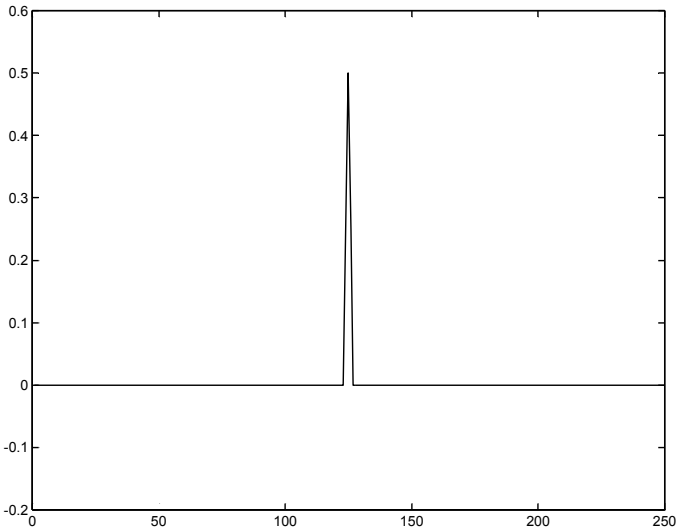


Figure 6
Impulse response of filter in ADM module

D/A processor
Before the single bit delta-sigma signal can be converted to analog an additional processing step is necessary to avoid non-linearity issues that are usually inherent in 1-bit conversions. With that the ADM then converts the signals to analog.

Analog low-pass filter
As the entire D/A converter has been designed with truthful transient response characteristic in mind, rather than any other standard design goal, special attention has been paid to the design of this analog output filter. To optimize sonic performance and transient response 2 gentle cascaded filters are applied to limit the high frequency noise.
As is commonly known the human ear can easily detect correlated signal components hidden in uncorrelated noise, and it is for this reason that the analog filters were not primarily designed to minimize the uncorrelated noise floor, but rather respond to the small signal transients that are so frequent and common with music signals. In other standard D/A converters more aggressive filter designs are used leading to similar effects as the pre-ringing explained in the upsampling paragraph of this data sheet, and also to other effects of clipped signal transients.
It is this particular analog low-pass filter design that contributes to the analog performance character of this converter.

Line stage output
The ADM module provides an internal dual differential line stage output that is designed to directly drive a

standard audio cable, be it balanced or unbalanced. The module does not provide any relay for output muting and it is recommended that one is added externally to mute each channel signal. The signal xMUTE_RLY on J3 can be used to control these external relays.

Pre-line stage outputs
If the designer wishes to use an external line stage, the module offers a choice of 2 separate pre-line stage outputs: either after the first analog filter (PL1 signal outputs) or after the second (PL2 signal outputs). A separate connector (J5, J6) for each channel is provided for these pre-line stage outputs, while the line stage output signals are provided on a 3rd connector (J4).

Power and ground considerations
The digital 12VD supply is very closely referenced to the analog circuitry on the module. While there are on-board regulators for the local digital circuitry this isolation may not be sufficient when the same 12VD supply is used for high power devices, especially when they are clocked, such as displays, motors etc.
Depending on the layout of the external power supply it may be necessary to provide a solid connection between the analog and digital grounds very close to the supply connectors (J3, J6).

Firmware update
From time to time AKDesign may make a special wave file available that contains a firmware update for the ADM. It can be played into the ADM as a regular audio file via any of its audio inputs. No audio will be audible during this operation. A power cycle will be necessary after completion of this operation in order to load the new program into active memory.
While playing this special wave file into the ADM the internal flash memory is erased, reprogrammed and verified. It is therefore vital that the process is not interrupted once it is started until the very end. The PrgrStat signals (see I2C bus definitions) indicate the status during programming. If the status signals indicate an error at the end the process can be restarted by first applying a reset to the ADM and then restarting the process again from the beginning. Under no circumstances should the power be turned off after an error occurred during programming or else the ADM will not be able to boot.
See section I2C bus definitions for more information.

I2C BUS DEFINITIONS

The ADM module communicates various states and controls via two separate and independent I2C buses (see pin description of digital connector):

- Host I2C Bus for external control of internal registers (requires external pullup resistors to 3.3V).
- Local I2C Bus for modules to display various states (pullup resistors on module) .

The purpose of the local I2C bus is to facilitate a simple user control interface allowing for display of basic internal states on a simple front panel without the need to use the Host I2C bus.

DEFINITIONS FOR HOST I2C BUS

The address of the module on the bus is: b00010xy whereby xy can be set by the user on the J3 digital connector pins 7,8. The module is slave on the bus.

Register write transfers always consist of 2 bytes: the first byte selects the register address and the second byte will be written into the data register pointed out by the first byte.
In order to read a register, a 1-byte write transfer has to be done first to set the register address. A second 1-byte read transfer will then read the register contents. If the same register is read multiple times no repeated write transfer will be necessary as the register address is memorized until changed.

Register Descriptions
To optimize sonic performance the ADM module should be polled as rarely as possible and ideally with a fundamental audio clock frequency (i.e. SCL should be derived from a frequency that is synchronous with the audio sample rate).

Audio Status (address 00000010)

7	6	5	4	3	2	1	0
STATE(3)	STATE(2)	STATE (1)	STATE (0)	EMPH	reserved	reserved	reserved
read-only	read-only	read-only	read-only	read-only			

The 4-bit STATE word indicates the detected sample rate:

0000: no lock, no signal
0001: 44.1kHz
0010: 48kHz
0011: 88.2kHz
0100: 96kHz
0101: 176.4kHz
0110: 192kHz
1001: 352.8kHz
1010: 384kHz
0111: DSD
1000: DSD 2X
1011: DSD 4X

EMPH (emphasis bit)

1 when emphasis bit detected in incoming AES data stream. Not valid when I2S input selected.

Audio Control (address 00000011)

7	6	5	4	3	2	1	0
reserved	SEL_INT	SEL_44	SEL_I2S	SEL_DSD	SEL_ I2CEN	PHASE	MUTE
	read/write	read/write	read/write	read/write	read/write	read/write	read/write
0	0	0	0	0	0	0	0*

SEL_INT (selection of master / slave clock operation, only valid when SEL_I2CEN=1)
1 selects master clock operation. In this mode the fundamental sample rate needs to be selected as well.
0 selects slave clock operation

SEL_44 (select fundamental sample rate, only valid when SEL_I2CEN=1 and SEL_INT=1)
1 sets the ADM configured in master clock mode to receive sample rates in multiples of 44.1kHz.
0 sets the ADM configured in master clock mode to receive sample rates in multiples of 48 kHz.

SEL_I2S (select AES input, only valid when SEL_I2CEN =1)
1 selects I2S input on module
0 selectsAES input on module (default after reset and power on).
Reading this bit will only give valid results when SEL_ I2CEN is set.

SEL_DSD (select DSD format on I2S input, only valid when SEL_ I2CEN =1)
1 selects DSD format on I2S input.
0 selects PCM format on I2S input (default after reset and power on).
Reading this bit will only give valid results when SEL_ I2CEN is set.

SEL_ I2CEN I2C control enable)
1 enables control of certain states via I2C control and disables hardware control.
0 disables I2C control. After each reset and power-on this bit is set to 0.

PHASE (phase inversion)
1 inverts phase of audio
0 no inversion

MUTE (mute audio output)
1 mutes audio output
0 unmute audio output

* default selection after reset or powerup.

Revision of ADM Module (address 00000100)

7	6	5	4	3	2	1	0
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
read-only	read-only	read-only	read-only	read-only	read-only	read-only	read-only

Indicates revision of ADM module (software).

Miscellaneous Status (address 00000101)

7	6	5	4	3	2	1	0
PrgrStat1	PrgrStat0	reserved	reserved	reserved	reserved	reserved	reserved
read-only	read-only						

The 2 PrgrStat bits indicate the status of the flash during programming:

00: normal operation

01: flash is being programmed (do not attempt any setup change or communication while this mode is active). From time to time AKDesign may make a special wave file available that contains a firmware update for the ADM. It can be played into the ADM as a regular audio file via any of its audio inputs. No audio will be audible during this operation. A power cycle will be necessary after completion of this operation in order to load the new program into active memory.

1x: an error occurred during the flash verification cycle. This condition can only be cleared with the xINIT hardware reset signal. If the power supply to the ADM is not turned off the old firmware is still active at this point. Therefore, a new firmware programming cycle should be started immediately after first asserting xINIT without turning off the power.

Temperature (address 00000110)

7	6	5	4	3	2	1	0
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
read-only	read-only	read-only	read-only	read-only	read-only	read-only	read-only

Indicates temperature of ADM module in Celsius. Format is 2's complement ranging from -128 to +127 degrees.

DEFINITIONS FOR LOCAL I2C BUS

This bus is primarily used for the ADM module to display its internal states via simple I2C bus ports. The module is bus master and sends out the following information every time a change has occurred:

Status (address 0100010, always 2 Bytes sent)
The address has been chosen so that a PCF8575TS port chip can be used to receive these 2 bytes.

First Byte:

7	6	5	4	3	2	1	0
PrgrStat1	PrgrStat0	reserved	reserved	bit3	bit2	bit1	EMPH

The 2 PrgrStat bits indicate the status of the flash during programming:

00: normal operation
01: flash is being programmed (do not attempt any setup change or communication while this mode is active). From time to time AKDesign may make a special wave file available that contains a firmware update for the ADM. It can be played into the ADM as a regular audio file via any of its audio inputs. No audio will be audible during this operation. A power cycle will be necessary after completion of this operation in order to load the new program into active memory.
1x: an error occurred during the flash verification cycle. This condition can only be cleared with the xINIT hardware reset signal. If the power supply to the ADM is not turned off the old firmware is still active at this point. Therefore, a new firmware programming cycle should be started immediately after first asserting xINIT without turning off the power.

Bit3, bit2 and bit1 are an extension of the second byte with the following meaning:

000: detected sample rate is indicated by second byte
001: 352.8kHz sample rate detected
010: 384kHz sample rate detected
100: DSD 4X

EMPH (emphasis bit)

This bit reflects the state of bit3 of the host audio status register (see host I2C bus register description).

Second Byte

7	6	5	4	3	2	1	0
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

The data byte indicates the detected sample rate. It is encoded so that individual LED's can be driven directly:

0000 0000: no lock, no signal
0000 0001: 44.1kHz
0000 0010: 48kHz
0000 0100: 88.2kHz
0000 1000: 96kHz
0001 0000: 176.4kHz
0010 0000: 192kHz
0100 0000: DSD
1000 0000: DSD 2X

MECHANICAL

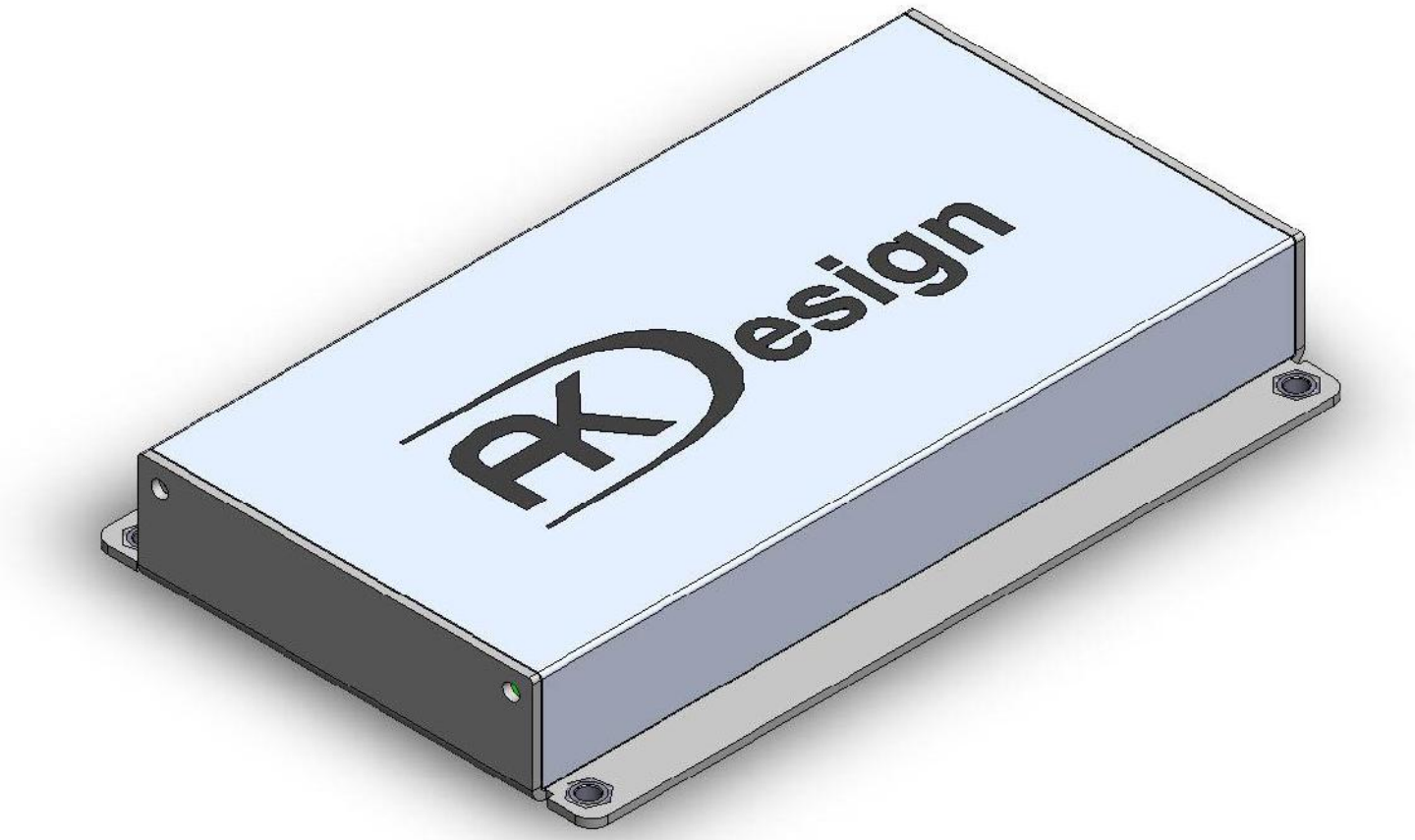
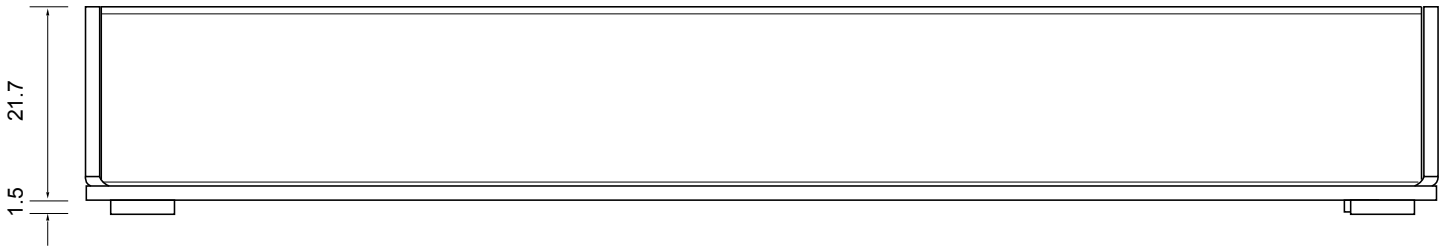
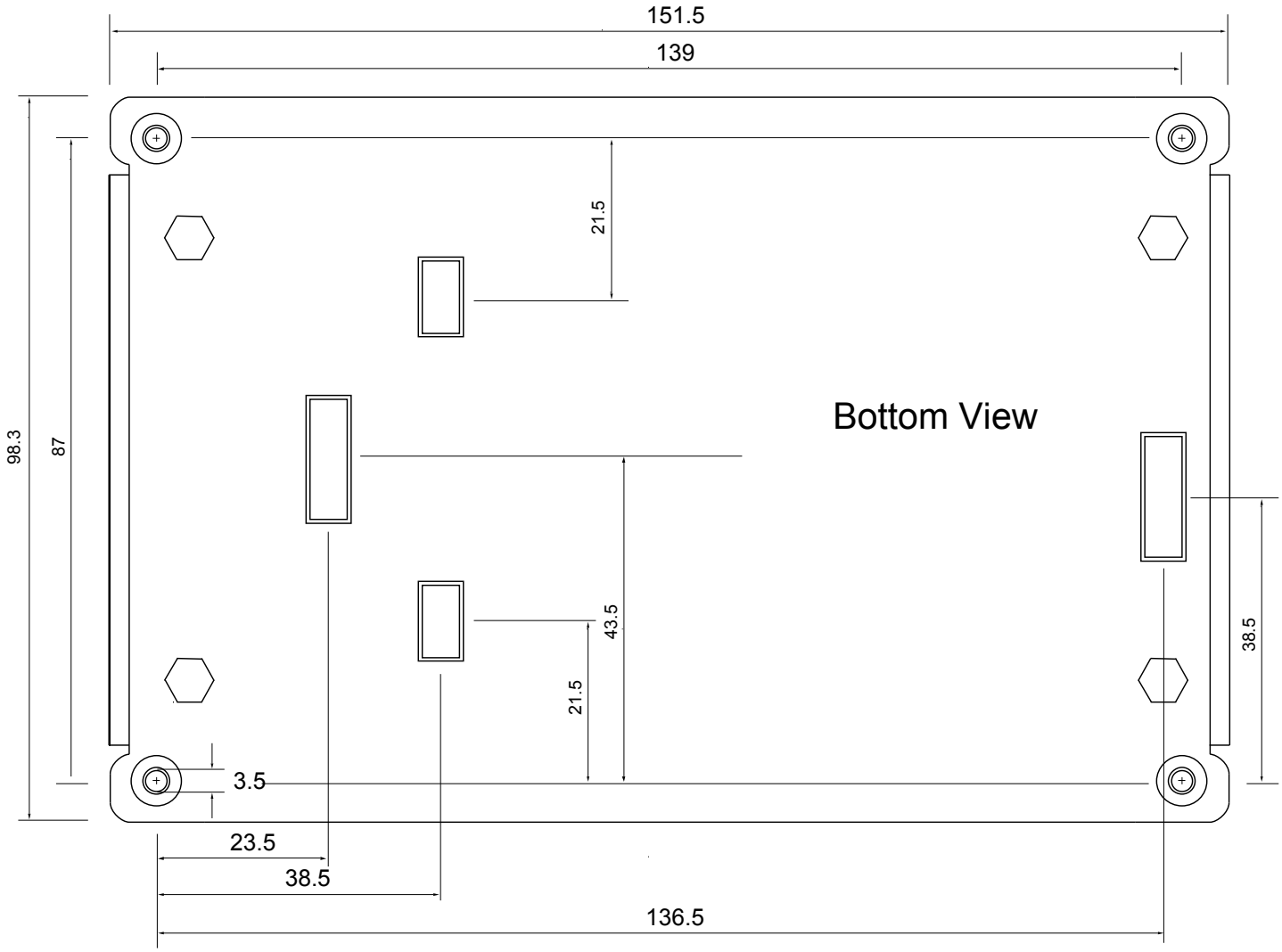


Figure 9 – Top view of module chassis

All dimensions are in mm.





REVISION HISTORY

June 14, 2013	Release
Aug. 21, 2013	Added firmware update feature.
April 11, 2014	Updated paragraphs I2S Receiver and Clock Generator
May 8, 2014	Added changes for support of DSD 4X, DoP via AES and I2S input, revised VD recommended figures